WHAT IS CLAIMED IS:

1. An apparatus for monitoring clock in a communication system for transmitting and receiving data, the apparatus comprising:

a first buffer block for receiving a synchronous signal and a clock from a system bus and temporarily storing the synchronous signal and clock ;

a first counter block for counting system clock using the synchronous signal as a reference;

a comparison block for latching a count value and comparing the count value to a reference value that is obtained from a normal operation;

a pulse generation block for generating a designated number of pulses when the count value is not equal to the reference value at a result of comparison;

a second counter block for counting a number of pulses generated by the pulse generation block during a monitoring cycle; and

a second buffer block for storing a count value obtained at the second counter block and clearing the count value when a system control block reads the count value.

2. The apparatus according to claim 1, wherein the first buffer block comprises an alternating current termination circuit for receiving the synchronous signal and the clock more stably.

3. The apparatus according to claim 1, wherein the first counter block receives the synchronous signal to a clear part of the first counter block.

4. The apparatus according to claim 1, wherein the comparison block latches the count value obtained from the first counter block right before the count value is cleared.

5. The apparatus according to claim 1, wherein the pulse generation block generates one pulse when the count value is not equal to the reference value.

6. The apparatus according to claim 1, wherein the pulse generation block does not generate pulse when the count value is equal to the reference value.

7. The apparatus according to claim 1, wherein the monitoring cycle of the second counter block is set to 2.5 seconds.

8. The apparatus according to claim 1, wherein the second buffer block stores the number of pulses generated until the control block reads the number.

9. The apparatus according to claim 1, wherein the system control block is a central processing unit.

10. The apparatus according to claim 1, further comprised of the first counter block determining the reference value according to the synchronous signal and clock.

11. A method for monitoring clock in a communication system for transmitting and receiving data, the method comprising:

receiving a synchronous signal and a clock from a system bus and temporarily storing the synchronous signal and clock by a first buffer block;

counting system clock using the synchronous signal as a reference by a first counter block;

latching a count value and comparing the count value to a reference value that is obtained from a normal operation by a comparison block;

generating a designated number of pulses when the count value is not equal to the reference value at a result of comparison by a pulse generation block;

counting a number of pulses generated by the pulse generation block during a monitoring cycle by a second counter block; and

storing a count value obtained at the second counter block and clearing the count value when a system control block reads the count value by a second buffer block.

12. The method according to claim 11, wherein the first buffer block comprises an alternating current termination circuit for receiving the synchronous signal and the clock more stably.

13. The method according to claim 11, wherein the first counter block receives the synchronous signal to a clear part of the first counter block.

14. The method according to claim 11, wherein the comparison block latches the count value obtained from the first counter block right before the count value is cleared.

15. The method according to claim 11, wherein the pulse generation block generates one pulse when the count value is not equal to the reference value.

16. The method according to claim 11, wherein the pulse generation block does not generate pulse when the count value is equal to the reference value.

17. The method according to claim 11, wherein the monitoring cycle of the second counter block is set to 2.5 seconds.

18. The method according to claim 11, wherein the second buffer block stores the number of pulses generated until the control block reads the number.

19. A computer-readable medium having computer-executable instructions for performing a method, comprising:

receiving a synchronous signal and a clock from a system bus and temporarily storing the synchronous signal and clock by a first buffer block;

counting system clock using the synchronous signal as a reference by a first counter block;

latching a count value and comparing the count value to a reference value that is obtained

from a normal operation by a comparison block;

generating a designated number of pulses when the count value is not equal to the reference value at a result of comparison by a pulse generation block;

counting a number of pulses generated by the pulse generation block during a monitoring cycle by a second counter block; and

storing a count value obtained at the second counter block and clearing the count value when a system control block reads the count value by a second buffer block.

20. A computer-readable medium having stored thereon a data structure comprising:

a first field containing data representing a first buffer block receiving a synchronous signal and clock from a system bus, and storing the synchronous signal and clock signal;

a second field containing data representing a first counter block receiving the system bus synchronous signal to a clear part of the first counter block of a counter, and counting a system clock using the synchronous signal as a reference, the first counter block determining the reference value according to the synchronous signal and clock;

a third field containing data representing a comparison block latching the count value right before the count value is cleared up, and comparing the value to a reference value obtained from a normal operation, and when the count value is the same as the reference value, the comparison block outputting '0' and when the count value is different from the reference value, the comparison block outputting '1';

a fourth field containing data representing a pulse generation block receiving the value '1'.

from the comparison block when the count value is not the same with the reference value, and generating a pulse and the pulse generation block receiving the value '0' from the comparison block when the count value is equal to the reference value, and does not generate a pulse;

a fifth field containing data representing a second counter block counting the number of pulses that are generated by the pulse generation block during monitoring cycle, and providing the result to the second buffer block; and

a sixth field containing data representing a second buffer block storing the count value provided by the second counter block, and simultaneously, as the system control block reads the value, the second buffer block clearing the value for monitoring during a next cycle;

a seventh field containing data representing the comparison block outputs the value '1' to the pulse generation block when the first counter block generating a value different from the reference value;

a eighth field containing data representing the pulse generator generating a pulse the moment the pulse generation block receives the value '1', and the second counter block counting the number of pulses generated at this time, during the monitoring cycle, the number of pulses generated by the pulse generation block is counted, and the counted number of pulses accommodates a detection of how many times the clock has been lost; and

a ninth field containing data representing the second buffer block storing the number of occurrences of clock loss, and the control block reading out the number and determining the present stability of clock of the system.